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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,557	03/12/2004	Santanu Chaudhuri	INTEL-0071	6472
34610 7590 05/04/2007 KED & ASSOCIATES, LLP P.O. Box 221200 Chantilly, VA 20153-1200			EXAMINER FLORES, LEON	
			ART UNIT 2611	PAPER NUMBER
			MAIL DATE 05/04/2007	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	Application No. 10/798,557	Applicant(s) CHAUDHURI ET AL.	
	Examiner Leon Flores	Art Unit 2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 12 March 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-30 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 17 June 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date <u>9/22/2005</u> | 6) <input type="checkbox"/> Other: _____  |

**DETAILED ACTION**

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claims (1-30) are rejected under 35 U.S.C. 102(b) as being anticipated by Dally (US Publication 2001/0026595 A1).**

Claim 1 is an apparatus claim corresponding to method claim 8. Hence, the steps performed in method claim 8 would have necessitated the elements in apparatus claim 1. Therefore, claim 1 has been analyzed and rejected w/r to claim 8.

Claim 2 is an apparatus claim corresponding to method claim 9. Hence, the steps performed in method claim 9 would have necessitated the elements in apparatus claim 2. Therefore, claim 2 has been analyzed and rejected w/r to claim 9.

Claim 3 is an apparatus claim corresponding to method claim 10. Hence, the steps performed in method claim 10 would have necessitated the elements in apparatus claim 3. Therefore, claim 3 has been analyzed and rejected w/r to claim 10.

Claim 4 is an apparatus claim corresponding to method claim 11. Hence, the steps performed in method claim 11 would have necessitated the elements in apparatus claim 4. Therefore, claim 4 has been analyzed and rejected w/r to claim 11.

Claim 5 is an apparatus claim corresponding to method claim 17. Hence, the steps performed in method claim 17 would have necessitated the elements in apparatus claim 5. Therefore, claim 5 has been analyzed and rejected w/r to claim 17.

Claim 6 is an apparatus claim corresponding to method claim 18. Hence, the steps performed in method claim 18 would have necessitated the elements in apparatus claim 6. Therefore, claim 6 has been analyzed and rejected w/r to claim 18.

Claim 7 is an apparatus claim corresponding to method claim 19. Hence, the steps performed in method claim 19 would have necessitated the elements in apparatus claim 7. Therefore, claim 7 has been analyzed and rejected w/r to claim 19.

Re claim 8, Dally discloses a method, comprising: measuring loss in a link between a transmitter and a receiver (See paragraphs 51-53); and automatically determining a multi-tap equalization setting for the transmitter based on the measured loss. (See paragraphs 51-53)

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Re claim 9, the reference of Dally further discloses that wherein the equalization setting is a two-tap coefficient setting. (See paragraph 45)

Re claim 10, the reference of Dally further discloses that wherein the equalization setting is a five-tap coefficient setting. (See paragraph 36)

Re claim 11, the reference of Dally further discloses that wherein measuring the loss is performed at the receiver. (See paragraph 52-53)

Re claim 12, the reference of Dally further discloses that wherein measuring the loss includes: transmitting a clock signal from the transmitter to the receiver (See paragraphs 51); and computing the loss as a ratio of the transmitted clock signal amplitude and the received clock signal amplitude. (See paragraphs 51-53)

Re claim 13, the reference of Dally further discloses that wherein the receiver receives the clock signal through an input which is offset calibrated. (See paragraph 52)

Re claim 14, the reference of Dally further discloses that wherein the receiver sweeps the offset to determine the amplitude of the received clock signal to within a predetermined error. (See paragraph 52)

Re claim 15, the reference of Dally further discloses that wherein the predetermined error is one LSB error. (See paragraph 52)

Re claim 16, the reference of Dally further discloses that wherein the loss is measured based on the following equation:

$$\text{Loss(dB)} = -20 \log(N_{\text{sub.AC}}/N_{\text{sub.DC}}) * (V_{\text{sub.dc.sub..sub.--eq}}/V_{\text{sub.swing}})$$
 where  $N_{\text{sub.AC}}$  is a number of steps to determine the amplitude of the received clock signal,  $N_{\text{sub.DC}}$  is a number of steps to determine a voltage swing of a DC voltage transmitted to the receiver,  $V_{\text{sub.dc.sub..sub.--sub.eq}}$  is an equalized DC voltage, and  $V_{\text{sub.swing}}$  is the voltage swing. (See paragraph 52. Furthermore, one skilled in the art would know how to make and use this formula based tests performed at the receiving end.)

Re claim 17, the reference of Dally further discloses storing a look-up table that includes a plurality of tap coefficient settings in correspondence with a respective number of loss values, wherein determining the equalization setting includes searching the look-up table for a tap coefficient setting which corresponds to the measured loss and setting an equalizer in the transmitter based on the tap coefficient setting obtained from the search. (See paragraph 43-44 & 53)

Re claim 18, the reference of Dally further discloses that wherein measuring the loss and determining the multi-tap equalization setting are performed during link

initialization. (See paragraph 51-53)

Re claim 19, the reference of Dally further discloses measuring voltage and timing margins of an eye diagram at the receiver; and tuning the multi-tap equalization setting based on the voltage and timing margins. (See paragraph 32-33 & 51-53. It is inherent that the tap coefficients are adaptively updated based on channel characteristics. And these channel characteristics or taps are used in the equalizer to update its tap coefficients, thus providing compensation due to the dispersion or fading in the channel.)

Claim 20 is a system claim corresponding to method claim 8. Hence, the steps performed in method claim 8 would have necessitated the elements in system claim 20. Therefore, claim 20 has been analyzed and rejected w/r to claim 8.

Re claim 21, the reference of Dally further discloses that wherein the first circuit includes a chipset and the second circuit includes a CPU. (See paragraph 26 and claim 50)

Re claim 22, the reference of Dally further discloses that wherein the first circuit includes a chipset and the second circuit includes a memory. (See fig. 1 & paragraph 43)

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Re claim 23, the reference of Dally further discloses that wherein the memory is one of a RAM and a cache. (See paragraph 43)

Re claim 24, the reference of Dally further discloses that wherein the first circuit includes a memory and the second circuit includes a CPU. (See fig. 1 & paragraph 43.)

Re claim 25, the reference of Dally further discloses that wherein the first circuit includes a graphical interface and the second circuit includes at least one of a memory, CPU, and chipset. (These features are inherent when the system is a digital system.)

Claim 26 is a system claim corresponding to method claim 17. Hence, the steps performed in method claim 17 would have necessitated the elements in system claim 26. Therefore, claim 26 has been analyzed and rejected w/r to claim 17.

Claim 27 is a system claim corresponding to method claim 18. Hence, the steps performed in method claim 18 would have necessitated the elements in system claim 27. Therefore, claim 27 has been analyzed and rejected w/r to claim 18.

Claim 28 is a system claim corresponding to method claim 8 & 17. Hence, the steps performed in method claim 8 & 17 would have necessitated the elements in system claim 28. Therefore, claim 28 has been analyzed and rejected w/r to claim 8 &



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17. Furthermore, the system of Dally is digital-based system.

Claim 29 is a system claim corresponding to method claim 18. Hence, the steps performed in method claim 18 would have necessitated the elements in system claim 29. Therefore, claim 29 has been analyzed and rejected w/r to claim 18. Furthermore, the system of Dally is digital-based system.

Claim 30 is a system claim corresponding to method claim 19. Hence, the steps performed in method claim 19 would have necessitated the elements in system claim 30. Therefore, claim 30 has been analyzed and rejected w/r to claim 19. Furthermore, the system of Dally is digital-based system.

### ***Contact***


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leon Flores whose telephone number is 571-270-1201. The examiner can normally be reached on Mon-Fri 7-5pm Alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LF  
March 30, 2007

  
DAVID C. PAYNE  
SUPERVISORY PATENT EXAMINER